Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

In the Claims:

Please amend the claims as follows:

1. (Previously Presented) A memory, comprising:

an address bus operable to receive an external address during a data-transfer cycle;

an address counter operable to generate an internal address during the data-transfer cycle;

an address decoder coupled to the address counter;

a comparator coupled to the address bus and operable to compare the external address to a value; and

a control circuit coupled to the comparator and operable to terminate the data-transfer cycle based on the relationship between the external address and the value.

2. (Original) The memory of claim 1 wherein:

the address bus is operable to receive an external column address; and

the address counter is operable to generate an internal column address.

3. (Original) The memory of claim 1 wherein:

the address bus is operable to receive an initial external address and a subsequent external address; and

the address counter is operable to store the initial external address and to generate the internal address by varying the stored initial external address.

4. (Original) The memory of claim 1 wherein:

the address bus is operable to receive an initial external address and a subsequent external address; and

the address counter is operable to store the initial external address, to generate an initial internal address equal to the stored initial external address, and to generate a subsequent internal address by varying the stored initial external address.

5. (Original) The memory of claim 1 wherein:

the address bus is operable to receive an initial external address and a subsequent external address; and

the address counter is operable to store the initial external address, to generate an initial internal address equal to the stored initial external address, and to generate a subsequent internal address equal to the subsequent external address by varying the stored initial external address.

6. (Original) The memory of claim 1, further comprising:

a data buffer;

wherein the comparator is coupled to the address counter and is operable to compare the external address to the internal address; and

wherein the control circuit is coupled to the data buffer and is operable to enable the data buffer if the external address equals the internal address and to disable the data buffer if the external address does not equal the internal address.

7. (Original) The memory of claim 1, further comprising:

a data buffer;

a storage circuit operable to store a predetermined address;

wherein the comparator is coupled to the storage circuit and is operable to compare the external address to the predetermined address; and

wherein the control circuit is coupled to the data buffer and is operable to enable the data buffer if the external address does not equal the predetermined address and to disable the data buffer if the external address equals the predetermined address.

8. (Original) The memory of claim 1, further comprising:

a data buffer;

wherein the comparator is coupled to the address counter and is operable to compare the external address to the internal address; and

wherein the control circuit is coupled to the data buffer and the address counter and is operable to enable the counter if the external address equals the internal address and to disable the counter if the external address does not equal the internal address.

9. (Original) The memory of claim 1, further comprising:

a data buffer;

a storage circuit operable to store a predetermined address;

wherein the comparator is coupled to the storage circuit and is operable to compare the external address to the predetermined address; and

wherein the control circuit is coupled to the data buffer and the address counter and is operable to enable the counter if the external address does not equal the predetermined address and to disable the counter if the external address equals the predetermined address.

10. (Original) The memory of claim 1 wherein the data-transfer cycle comprises a read cycle.

11. (Previously Presented) A memory, comprising:

a data buffer operable to receive and hold data during a data-transfer cycle;

an address counter operable to generate an internal address during the data-transfer cycle;

a programmable storage circuit operable to store an address value during the data-transfer cycle;

a comparator coupled to the address counter and the storage circuit and operable to compare the internal address to the address value; and

a control circuit coupled to the storage circuit, the comparator, and the data buffer and operable to terminate the data-transfer cycle when the internal address has a predetermined relationship to the address value.

12. (Original) The memory of claim 11 wherein the control circuit is operable to disable the address counter in response to the value.

13. (Original) The memory of claim 11 wherein the control circuit is operable to disable the data buffer in response to the value.

14. (Previously Presented) The memory of claim 11 wherein:

the programmable storage circuit comprises a programmable counter operable to generate a count by incrementing or decrementing the stored value during the data-transfer cycle; and

wherein the control circuit is operable to terminate the data-transfer cycle when the count equals a predetermined value.

15. Cancelled.

16. (Original) The memory of claim 11 wherein the address counter is operable to generate an internal column address.

17. (Original) The memory of claim 11 wherein the address counter is operable to store an initial internal address and to generate a subsequent internal address by incrementing or decrementing the stored initial internal address.

18. (Original) An electronic system, comprising:

a data input device;

a data output device; and

a computer circuit coupled to the data input and output devices and including a processor and a memory circuit coupled to the processor, the memory circuit including,

an address bus operable to receive an external address from the processor during a data transfer between the processor and the memory,

an address counter operable to generate an internal address during the data transfer,

an address decoder, and

a multiplexer coupled to the address bus, the address counter, and the address decoder and operable to couple either the external address or the internal address to the address decoder during the data transfer.

19. (Original) The electronic system of claim 18 wherein the memory further includes:

wherein the multiplexer is operable to couple the internal address to the address decoder during the data transfer;

a comparator coupled to the address bus and the address decoder and operable to compare the external address to the internal address; and

a control circuit coupled to the comparator and operable to enable the data transfer if the external address equals the internal address and to disable the data transfer if the external address does not equal the internal address.

20. (Previously Presented) An electronic system, comprising:

a data input device;

a data output device; and

a computer circuit coupled to the data input and output devices and including a processor and a memory circuit coupled to the processor, the memory circuit including,

an address counter operable to generate an internal address during a data–transfer cycle between the processor and the memory;

a storage circuit operable to receive and store an address value from the processor before or during the data-transfer cycle;

a comparator coupled to the address counter and the storage circuit and operable to compare the internal address to the address value; and

a control circuit coupled to the storage circuit and the comparator and operable to terminate the data–transfer cycle when the internal address has a predetermined relationship to the address value.

21. (Previously Presented) The electronic system of claim 20 wherein:

the storage circuit comprises a programmable counter operable to generate a count by incrementing or decrementing the stored value during the data–transfer cycle; and

wherein the control circuit is operable to terminate the data-transfer when the count equals a predetermined value.

22. Cancelled.

23. (Currently Amended) A method, comprising:

receiving a first address during a data-transfer cycle;

generating a second address during the data-transfer cycle;

comparing the first address to the second address; and

terminating ~~a~~ the data-transfer cycle during which data is being transferred to or from a storage location residing at the second address if the first address does not have a predetermined relationship to the second address.

24. (Previously Presented) The method of claim 23, further comprising enabling the cycle if the first address has the predetermined relationship to the second address.

25. (Original) The method of claim 23 wherein:

receiving a first address comprises receiving with a memory circuit a first address that is generated outside of the memory circuit; and

generating a second address comprises generating a second address inside of the memory circuit.

26. (Previously Presented) The method of claim 23, further comprising:

wherein terminating the cycle comprises terminating the cycle if the address does not equal the second address; and

enabling the cycle if the first address equals the second address.

27. (Currently Amended) A method, comprising:

generating a first address during a data-transfer cycle;

comparing the first address to a predetermined value; and

terminating ~~a~~ the data-transfer cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value.

28. (Previously Presented) The method of claim 27, further comprising enabling the cycle if the first address does not have the predetermined relationship to the predetermined value.

29. (Original) The method of claim 27 wherein generating a first address comprises generating the first address inside of a memory circuit.

30. (Original) The method of claim 27 wherein generating a first address comprises generating the first address outside of a memory circuit.

31. (Previously Presented) The method of claim 27, further comprising:

wherein disabling the cycle comprises disabling the cycle if the first address equals the predetermined value; and

enabling the cycle if the first address does not equal the predetermined value.

32. (Original) The method of claim 27, further comprising:

wherein generating a first address comprises generating the first address inside of a memory circuit; and

receiving with the memory circuit a second address from outside of the memory circuit.

33. (Original) The method of claim 27, further comprising loading the predetermined value into a memory that includes the storage location.

34. (Previously Presented) A method, comprising:

loading a memory with a count value from an external source;

generating a first address inside of the memory, the first address being distinct from the count value;

incrementing or decrementing the count value;

comparing the count value to a predetermined value; and

terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the count value has a predetermined relationship to the predetermined value.

35. (Previously Presented) The method of claim 34, further comprising enabling the cycle if the first address does not have the predetermined relationship to the predetermined value.

36. (Previously Presented) The method of claim 34, further comprising:

wherein terminating the cycle comprises terminating the cycle if the count value equals the predetermined value; and

enabling the cycle if the count value does not equal the predetermined value.

37. (Original) The method of claim 34, further comprising receiving with the memory a second address from outside of the memory while generating the first address.

38. (Previously Presented) A memory, comprising:

an address bus operable to receive an external address during a data-transfer cycle;

an address counter operable to generate an internal address during the data-transfer cycle;

an address decoder coupled to the address counter;

a comparator coupled to the address bus and to the address counter and operable to compare the external address to the internal address;

a control circuit coupled to the comparator and operable to enable a data transfer based on the relationship between the external address and the internal address.

39. (Previously Presented) A memory, comprising:

a data buffer operable to receive and hold data during a data-transfer cycle;

an address counter operable to generate an internal address during the data-transfer cycle;

a programmable storage circuit operable to store a value during the data-transfer cycle; and

a control circuit coupled to the storage circuit and the data buffer and operable to terminate the data-transfer cycle in response to the value.

40. (Previously Presented) An electronic system, comprising:

a data input device;

a data output device; and

a computer circuit coupled to the data input and output devices and including a processor and a memory circuit coupled to the processor, the memory circuit including,

an address counter operable to generate an internal address during a data–transfer cycle between the processor and the memory;

a storage circuit operable to receive and store a value from the processor before or during the data-transfer cycle; and

a control circuit coupled to the storage circuit and operable to terminate the data–transfer cycle in response to the stored value.